ABSTRACT

The present invention relates generally to photolithographic systems and methods, and more particularly to systems and methodologies that facilitate the reduction of line-edge roughness (LER) during gate formation in an integrated circuit.

Systems and methods are disclosed for improving critical dimension (CD) of photoresist lines, comprising a non-lithographic shrink component that facilitates mitigating LER, and a trim etch component that facilitates achieving and/or restoring a target critical dimension.